24 22
58. (New) The non-volatile memory array of claim 56, and wherein said conductive member includes polysilicon.

25 24
59. (New) The non-volatile memory array of claim 58, and wherein said conductive member includes a metal silicide.

26 24
60. (New) The non-volatile memory array of claim 58, and wherein said conductive member includes a metal.--

REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow.

In the February 27, 2001, Office Action in this application, the Examiner rejected Applicants' claims 1-9 under 35 U.S.C. §103(a) as being unpatentable over the Sung et al. reference in view of the Lee reference.

As indicated above, Applicants' claims 1-9 have been cancelled in favor of new claims 35-43. For the reasons set forth below, Applicants traverses the §103(a) rejection based upon the Sung et al./Lee reference combination as applied to new claims 35-43.

More specifically, as recited in Applicants' new independent claim 35, the present invention is directed to a non-volatile memory array that includes a plurality of memory cells arranged in rows and columns in a semiconductor substrate. As is typical in non-volatile memory arrays, each of the memory cells includes a drain region, a source region, and a channel region disposed between the drain region and the source region. In accordance with the present invention, and as recited in Applicants' new independent claim 35, a conductive member disposed along at least a portion of each row of memory cells in the array. The conductive member makes electrical contact with the source regions of the memory cells in that portion of the row. Furthermore, the conductive member is self-aligned with the memory cells of that portion of the row.

As stated in Applicants' specification on page 6, beginning in line 27, unlike the prior art, the source regions of the memory cells in adjacent columns of the non-volatile memory array of the present invention remain isolated, on the substrate level, by dielectric isolation regions formed in the semiconductor substrate. As further stated in Applicants' specification, although the source regions are electrically isolated from one another on the substrate level, the source regions are commonly connected by low resistance source conductor members formed after the memory cells. This structure, as stated in Applicants' Summary of the Invention section of the application, improves cell endurance, provides for low supply voltage operation and reduces cell current variations during programming and erase operations. Furthermore, the structure reduces the number of source contacts required in the array.

In this regard, the Sung et al. reference is representative of the prior art, which does not include electrical isolation between the source regions of adjacent columns of memory cells. That is, the Sung et al. reference does not teach that sources corresponding to several word lines can be arbitrarily connected in any combination. While the Sung et al. patent discloses processing techniques that are potentially capable of generating the claimed structure, the teaching of individual process steps does not either teach or suggest that these steps may be combined in a particular way to arrive at a particular device structure, particularly the non-volatile memory array structure defined by Applicants' new independent claim 35. Thus, it is submitted that new independent claim 35, and all claims depending therefrom, patentably distinguish over the Sung et al./Lee combination.

Since the Sung et al. reference provides the primary basis for the rejection of all claims in this application, and since each of Applicants' new independent claims, i.e., claim 35, claim 47, and claim 56, recite that the source regions of adjacent columns of memory cells of the claimed non-volatile memory array are electrically isolated by dielectric isolation regions formed in the semiconductor substrate, and since this feature is neither taught nor suggested by any of the references considered individually or in combination, it is submitted that all claims now pending in this application patentably distinguish over the prior art.

For the reasons set forth above, it is requested that this application be passed to allowance.

Respectfully submitted,

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